Amendments to the Specification:

Please amend the paragraph beginning on page 9, line 15 as follows:

--An embodiment of the instant invention for a SOI dynamic logic circuit is illustrated in Figure 4. This embodiment has an output logic function of $\overline{A \bullet B}$ and logic inputs of A 230 and B 240. The precharge circuit which comprises a PMOS transistor 210 and the ground switch circuit which comprises a NMOS transistor 220 are connected to a clock signal 235. Although both 210 and 220 are shown tied to the same clock signal 235 it is possible to have independent clock signals driving either transistor. In this embodiment the PDN 260 comprises a series connection of a PMOS transistor 270 and a NMOS transistor 280. In a further embodiment one of the transistors in the PDN 260 has the gate tied to the floating substrate 330. During the precharge phase (when the clock 235 is low) the output node 250 will be charged high to approximately V_{DD} 290 through the PMOS precharge transistor 210. During the subsequent discharge or logic phase (when the clock 235 is high) if logic input A 230 is low and logic input B 240 is high the output node 250 will be pulled-down by the PDN 260 to a value close to the circuit ground 300. The transistors 270 and 280 thus provide a potential conductive path from the output node 250 to the circuit ground 300. This is to be contrasted with a bulk CMOS circuit implementing the same logic function where the PDN comprises NMOS transistors. The circuit of Figure 4 can be extended to any number of series connected PMOS and NMOS transistors in the PDN 260. In addition, the circuit shown in Figure 4 could be a subset of a larger circuit. Thus logic inputs A 230 and B 240 could be provided by addition circuitry 262 and the logic output 250 could be connected to the other circuits 264.--

Please amend the paragraph beginning on page 10, line 10 as follows:

-- Another embodiment of the instant invention for a SOI dynamic logic circuit is illustrated in Figure 5. This embodiment has an output logic function of $A+B$ and logic inputs of A 230 and B 240. The precharge PMOS transistor 210 and the NMOS ground

switch transistor 220 are connected to a clock signal 235. Although both 210 and 220 are shown tied to the same clock signal 235 it is possible to have independent clock signals driving either transistor. In this embodiment the PDN 265 comprises a series connection of PMOS transistors 272 and 282. In a further embodiment one of the transistors in the PDN 265 has the gate tied to the floating substrate 320. During the precharge phase (when the clock 235 is low) the output node 252 will be charged high to approximately V_{DD} 290 through the PMOS precharge transistor 210. During the subsequent discharge or logic phase (when the clock 235 is high) if both logic inputs A 230 and B 240 are low the output node 250 will be pulled-down by the PDN 265 to a value close to the circuit ground 300. The transistors 272 and 282 thus provide a potential conductive path from the output node 252 to the circuit ground 300. This is to be contrasted with a bulk CMOS circuit implementing the same logic function where the PDN comprises NMOS transistors. The circuit of Figure 5 can be extended to any number of series connected PMOS transistors in the PDN 265. In addition, the circuit shown in Figure 5 could be a subset of a larger circuit. Thus logic inputs A 230 and B 240 could be provided by addition circuitry 262 and the logic output 250 could be connected to the other circuits 264.--

Please amend the paragraph beginning on page 11, line 6 as follows:

--An further embodiment of the instant invention for a SOI dynamic logic circuit is illustrated in Figure 6. This embodiment has an output logic function of $\overline{\overline{A}+B}$ and logic inputs of A 230 and B 240. The precharge PMOS transistor 210 and the NMOS ground switch transistor 220 are connected to a clock signal 235. Although both 210 and 220 are shown tied to the same clock signal 235 it is possible to have independent clock signals driving either transistor. In this embodiment the PDN 266 comprises a parallel connection of a PMOS transistor 274 and a NMOS transistor 284. In a further embodiment one of the transistors in the PDN 266 has the gate tied to the floating substrate 340. This parallel connection results in a pair of common circuit nodes 302 and 304. Circuit node 302 is connected to the output node 254 and the precharge

transistor 210. Circuit node 304 is connected to the ground switch transistor 220. During the precharge phase (when the clock 235 is low) the output node 254 will be charged high to approximately V_{DD} 290 through the PMOS precharge transistor 210. During the subsequent discharge or logic phase (when the clock 235 is high) if either logic input A 230 is low or logic input B 240 is high, the output node 254 will be pulled-down by the PDN 266 to a value close to the circuit ground 300. The transistors 274 and 284 thus provide a potential conductive path from the output node 254 to the circuit ground 300. This is to be contrasted with a bulk CMOS circuit implementing the same logic function where the PDN comprises NMOS transistors. The circuit of Figure 6 can be extended to any number of parallel connected PMOS and NMOS transistors in the PDN 266. In addition, the circuit shown in Figure 6 could be a subset of a larger circuit. Thus logic inputs A 230 and B 240 could be provided by addition circuitry 262 and the logic output 250 could be connected to the other circuits 264.--